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10/706,419	11/12/2003	Paul D. Stultz	016295.1471	6796

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,419	STULTZ, PAUL D.	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodman et al (US6282601) hereinafter Goodman in view of Narad et al (US5692197) hereinafter Narad.

3. As to claim 1, Goodman discloses an information handling system, comprising: a plurality of processors coupled to a processor bus (Goodman teaches in figure 1 of a plurality of processors 12a, 12b ...12n, COL. 3, lines 1 - 10); and

a memory (a system memory 16 in figure 1, COL. 3, lines 1 - 10);

Goodman does not explicitly teach wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode.

However, Narad teaches wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is

associated with each processor and indicates whether the associated processor has exited the interrupt mode.

Narad teaches in figure 1A of a multiple computer system (110, 120,...170). This computer system comprises a system controller that comprises semaphores associated with each computer node that indicate the state of said computer, whether it is in the sleep mode or the power-down mode, COL. 4, lines 8 – 22.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Goodman and Narad to manage the power consumption of a computer system, COL. 1, line 65 – COL. 2, line 9.

The combination would have been obvious because one of ordinary skill in the art would want to manage the individual computer power savings in the system, (COL. 2, lines 10 – 20).

4. As to claim 2, Goodman discloses the information handling system, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (the semaphores are stored in register file 78 of figure 2 in unique multiple subsets, COL. 4, lines 10 – 18).

5. As to claim 3, Goodman discloses the information handling system, wherein each processor is operable to access the semaphore associated with the other processors of the information handling system (a predetermined signature for each

processor is stored in the SMI memory register 78 and is read-accessible, COL. 4, lines 9 – 10).

6. As to claim 4, Goodman discloses the information handling system, wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis (each process has said access to register 78 that comprises the semaphores, COL. 4, lines 9 – 10).

7. As to claim 5, Goodman discloses the information handling system, wherein the memory location associated with the storage of the semaphores associated with the processors of the information handling system is memory space dedicated to storing data associated with the entry of the processors into interrupt mode (said memory space allocation for interrupt sequences, such as power-on self test, COL. 4, lines 10 – 18).

8. As to claim 6, Goodman discloses the information handling system, wherein the interrupt mode is system management interrupt mode (the interrupt mode is said mode, COL. 3, lines 42 – 45).

9. As to claim 7, Goodman discloses the information handling system of claim 1, wherein the interrupt mode is system management interrupt mode; wherein the semaphore associated with a processor is stored in a memory location that is offset

from a base memory location by a unique offset indicator associated with the processor (the semaphores are stored in register file 78 of figure 2 in unique multiple subsets, COL. 4, lines 10 – 18); and

wherein each processor is operable to access the semaphore associated with the other processors of the information handling system on a non-exclusive basis (each process has said access to register 78 that comprises the semaphores, COL. 4, lines 9 – 10).

10. As to claim 8, Goodman discloses a method for processing an interrupt in a multiple processor computer system, comprising the steps of: for each processor, entering interrupt mode (each processor enters the interrupt mode from the assertion of an SMI interrupt to all processors, COL. 4, lines 54 – 56);

Narad teaches for each processor, setting a semaphore associated with the processor to indicate that the processor has exited the interrupt mode, wherein a uniquely addressable semaphore is associated with each processor (a multiple computer system (110, 120,... 170) is illustrated in figure 1A. This computer system comprises a system controller that comprises semaphores associated with each computer node that indicate the state of said computer, whether it is in the sleep mode or the power-down mode, COL. 4, lines 8 – 22); and

Narad teaches for each non-interrupt handling processors, exiting interrupt mode up following the negation of the semaphore associated with the processor (a wakeup request is asserted that clears the semaphore bit, causing the computer to be powered up, COL. 2, lines 55 - 67).

11. As to claim 9, Goodman discloses the method for processing an interrupt in a multiple processor computer system, wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis (a multiple processor system includes the step of setting a semaphore for each processor by interrupting all processors, COL. 4, lines 54 - 56).

12. As to claim 10, Goodman discloses the method for processing an interrupt in a multiple processor computer system, wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (said step in step 128 of figure 4, where a comparison of the semaphore of each processor is checked against that of the request of the interrupt hardware).

13. As to claim 11, Goodman discloses the method for processing an interrupt in a multiple processor computer system of claim 8, wherein the interrupt is a system management interrupt (the interrupt mode is said mode, COL. 3, lines 42 – 45).

14. As to claim 12, Goodman discloses the method for processing an interrupt in a multiple processor computer system of claim 8, wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique

offset indicator (the semaphores are stored in register file 78 of figure 2 in unique multiple subsets, COL. 4, lines 10 – 18).

15. As to claim 13, Goodman discloses the method for processing an interrupt in a multiple processor computer system of claim 8, wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis (a multiple processor system includes the step of setting a semaphore for each processor by interrupting all processors, COL. 4, lines 54 - 56);

wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (said step in step 128 of figure 4, where a comparison of the semaphore of each processor is checked against that of the request of the interrupt hardware); and

wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique offset indicator (the semaphores are stored in register file 78 of figure 2 in unique multiple subsets, COL. 4, lines 10 – 18).

16. As to claim 14, Goodman discloses the method for processing an interrupt in a multiple processor computer system of claim 8, wherein the interrupt is a system management interrupt (Goodman teaches of the interrupt mode is said mode, COL. 3, lines 42 – 45);

wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis; wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (a multiple processor system includes the step of setting a semaphore for each processor by interrupting all processors, COL. 4, lines 54 - 56); and

wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (the semaphores are stored in register file 78 of figure 2 in unique multiple subsets, COL. 4, lines 10 – 18).

17. As to claim 15, Goodman discloses a computer system, comprising: a plurality of processors;

a memory (figure 1 of a plurality of processors 12a, 12b ... 12n, COL. 3, lines 1 - 10);

a memory (a system memory 16 in figure 1, COL. 3, lines 1 - 10);

wherein the architecture of the processors and the memory is a non-uniform memory access architecture (the support other multiple computer systems comprising numa architecture machines , COL. 2, lines 55 – 67); and

Narad teaches wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode (a multiple computer system (110, 120,... 170). This computer system comprises

a system controller that comprises semaphores associated with each computer node that indicate the state of said computer, whether it is in the sleep mode or the power-down mode, COL. 4, lines 8 – 22).

18. As to claim 16, Goodman discloses the computer system of claim 15, wherein the interrupt mode is associated with a system management interrupt (the interrupt mode is said mode, COL. 3, lines 42 – 45).

19. As to claim 17, Goodman discloses the computer system of claim 16, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (the semaphores are stored in register file 78 of figure 2 in unique multiple subsets, COL. 4, lines 10 – 18).

20. As to claim 18, Goodman discloses the computer system of claim 17, wherein the memory location associated with the storage of the semaphores is memory space dedicated to storing data associated with the entry of the processors into interrupt mode (said memory space allocation for interrupt sequences, such as power-on self test, COL. 4, lines 10 – 18).

21. As to claim 19, Goodman discloses the computer system of claim 16, wherein the semaphores may be accessed by each of the processors on a non-exclusive basis

(each process has said access to register 78 that comprises the semaphores, COL. 4, lines 9 – 10).

22. As to claim 20, Goodman discloses the computer system of claim 16, wherein the semaphores may be accessed by each of the processors on a non-exclusive basis (each process has said access to register 78 that comprises the semaphores, COL. 4, lines 9 – 10); and

wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (the semaphores are stored in register file 78 of figure 2 in unique multiple subsets, COL. 4, lines 10 – 18).

Response to Arguments

23. Applicant's arguments with respect to claims 1,8, and 15 have been considered but are moot in view of the new ground(s) of rejection. With regard to the applicant's argument that the amended claim's limitation that Goodman does not disclose a uniquely addressable semaphore associated with each processor to indicate whether the associated processor has exited the interrupt mode. The office points to the teaching of Narad illustrating in figure 1A, a multiple computer system (110, 120,... 170). This computer system comprises a system controller that comprises unique semaphores associated with each computer node that indicate the state of said computer, whether it is in the sleep mode or the power-down mode, (COL. 4, lines 8 – 22).

24.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571 272 3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD
1/29/2006

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1/30/06